Tools & Hardware

This independent study focused heavily on High-Level Synthesis (HLS) using Xilinx Vitis, with Vivado used primarily for block design and integration. Vitis allowed us to write hardware-accelerated logic in C/C++ and synthesize it into IP blocks, which we then connected using Vivado's IP integrator.

We deployed our designs on two FPGA development boards:

- **Zybo Z20:** Our primary platform,for working with AXI peripherals and DMA.
- **PYNQ-Z1:** Useful for testing Python-controlled overlay.

Resources Used

HLS & System Design

- Synthesis of High-Level Synthesis textbook – our main reference for learning HLS concepts, dataflow optimization, and pipelining strategies.
- AMD Vitis Streaming IP Tutorial – helpful for creating streaming IPs and understanding HLS/Vitis workflows.

PYNQ Overlays

- Overlay Customization
- Loading Overlays
  These were essential for learning how to deploy and interact with hardware overlays using Python on the PYNQ-Z1.

Zybo Labs & AXI/DMA Integration

- Programming Projects for FPGAs – we used this extensively for hands-on labs on AXI streaming, DMA, and HLS.
- AXI DMA Tutorial – specifically helped us configure DMA on the Zybo.
- Zybo Tutorial & Vivado RTL Intro – additional references during early setup and debugging.

PMod OLED Integration

- PMod OLED Reference Manual – used to get the OLED peripheral working on the Zybo. Code was included in the final deliverables to Dr. Picone.

Chess Engine Exploration

- AlphaZero (Python/Keras) – inspired early ideas for accelerated game engines.
- Stockfish NNUE – reviewed for insights into optimized evaluation and neural net integration.