Name: _____

Problem	Points	Score
1a	10	
1b	10	
1c	10	
1d	10	
2a	10	
2b	10	
2c	10	
3a	10	
3b	10	
3c	10	
Total	**100**	

Notes:

1. The exam is closed book / closed notes. Students are allowed a copy sheet — only **one** side of **one** standard US-size (8.5” x 11”) sheet of paper — on which they can write relevant information such as theorems.

2. Please show ALL work. Incorrect answers with no supporting explanations or work will be given no partial credit.

3. If I can’t read or follow your solution, it is wrong, and no partial credit will be given — PLEASE BE NEAT!

4. Please indicate clearly your answer to every problem.

5. There is sufficient space after each problem to write your solution. In case you need extra paper please see the instructor.

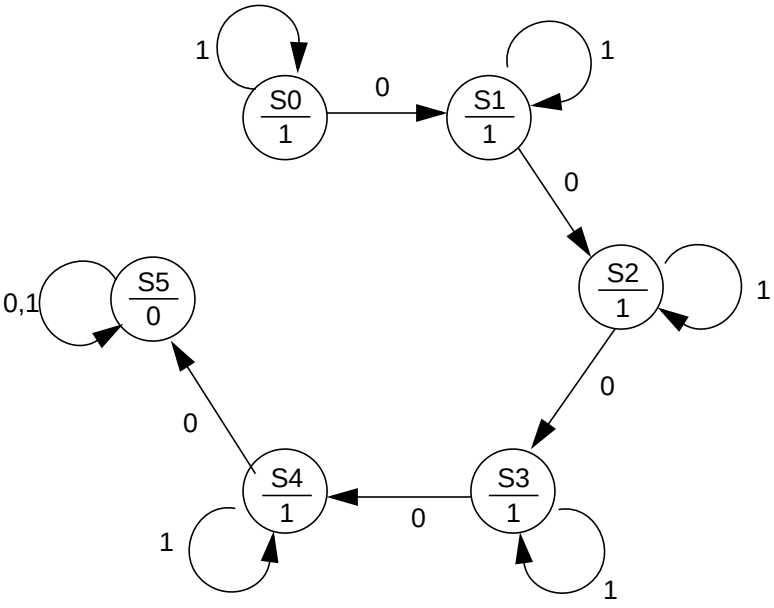
6. Calculators of any kind are not allowed.

Problem No. 1:

An alarm system is designed to trigger on iff the number of unsuccessful password entries is 5 or more. An iterative sequential network is used to keep track of the entries, where every cell of the network records one password entry. An unsuccessful attempt is input as $X_i = 0$, a successful attempt is input as $X_i = 1$. The alarm is turned on when the final output of the network is $Z_n = 0$.

a) Draw the state graph of a Moore network to implement a typical cell of the iterative network. Draw the corresponding state table.

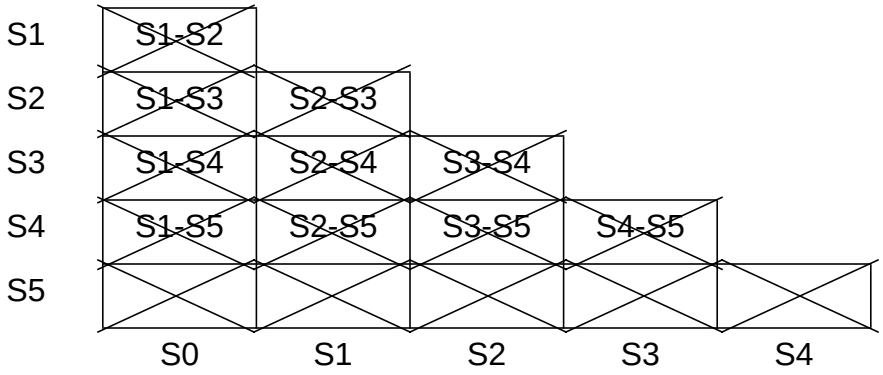
Solution:



Curr. state	Next state		Z
	X=0	X=1	
S0	S1	S0	1
S1	S2	S1	1
S2	S3	S2	1
S3	S4	S3	1
S4	S5	S4	1
S5	S5	S5	0

b) Use the implication chart method to identify equivalent states. Remove redundant states and draw the minimum state table.

Solution:



Thus no two states are equivalent. This is the minimum state representation of the state table.

c) Using the three guidelines for state assignment, assign the states in an optimal fashion.

Solution:

By the first guideline (states that have the same next states for a particular input should be placed together) we get —

S4, S5

By the second guideline (states that are the next states of a state should be placed together) we get —

S0,S1 S1, S2
S2, S3 S3, S4
S4, S5

By the third guideline (states that have the same output should be placed together) we get —

S0, S1, S2, S3, S4

One possible state assignment is then —

C \ AB	00	01	11	10
0	S0			S5
1	S1	S2	S3	S4

$A_iB_iC_i$	$A_{i+1}B_{i+1}C_{i+1}$		Z
	X=0	X=1	
000	001	000	1
001	011	001	1
011	111	011	1
111	101	111	1
101	100	101	1
100	100	100	0

d) Draw the K-maps and derive the equations for a typical cell for the alarm system.

Solution:

BC \ XA	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	1	1	0
10	X	X	X	X

$$A_{i+1} = A_i + X'_i B_i$$

BC \ XA	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	0	1	1
10	X	X	X	X

$$B_{i+1} = X'_i A'_i C_i + X_i B_i$$

BC \ XA	00	01	11	10
00	1	0	0	0
01	1	0	1	1
11	1	1	1	1
10	X	X	X	X

$$C_{i+1} = B_i + X_i C_i + X'_i A'_i$$

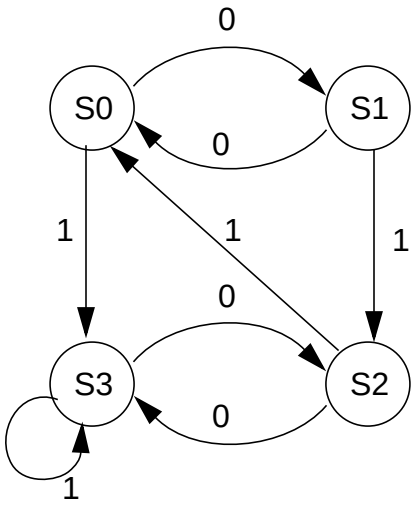
C \ AB	00	01	11	10
0	1	X	X	0
1	1	1	1	1

$$Z_n = C_n + A'_n$$

Problem No. 2:

The 74S163 4-bit synchronous counter has the following function table —

Control Signals			Next State			
CLEAR	**LOAD**	**PT**	Q_D^+	Q_C^+	Q_B^+	Q_A^+
0	X	X	0	0	0	0
1	0	X	D_D	D_C	D_B	D_A
1	1	0	Q_D	Q_C	Q_B	Q_A
1	1	1	present state + 1			



The network described by the adjacent state graph is to be implemented using a 74S163 counter and external logic gates.

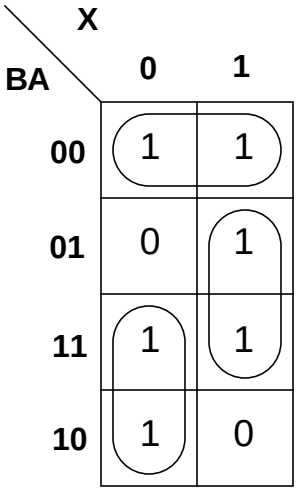
a) Draw the next-state table to derive the counter inputs to implement the adjacent state graph.

Solution:

	BA	B^+A^+	**74S163 Input Variables**			
			Clear	**Load**	D_BD_A	**PT**
X=0	00	01	1	1	XX	1
	01	00	0	X	XX	X
	10	11	1	1	XX	1
	11	10	1	0	10	X
X=1	00	11	1	0	11	X
	01	10	1	1	XX	1
	10	00	0	X	XX	X
	11	11	1	1	XX	0

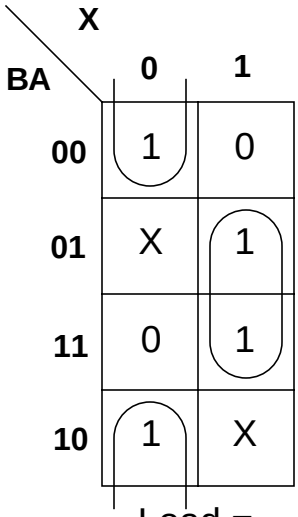
b) Draw the K-maps and derive equations for the counter inputs.

Solution:



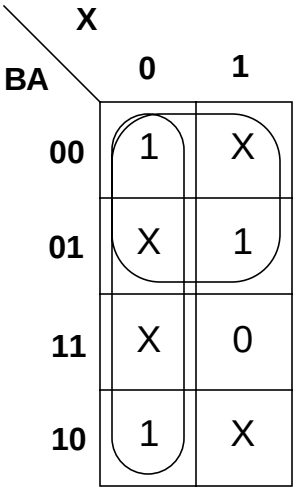
Clear =

B'A' + XA + X'B



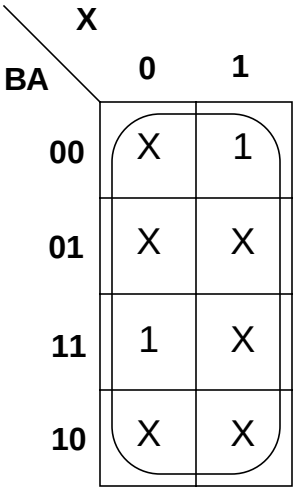
Load =

X'A' + XA



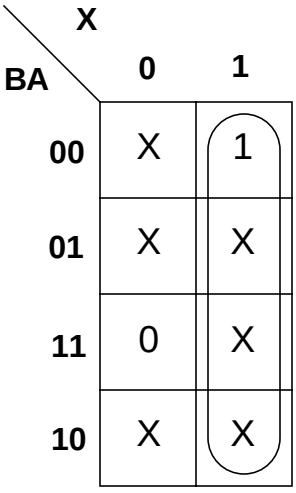
PT =

X' + B'



D_B =

1

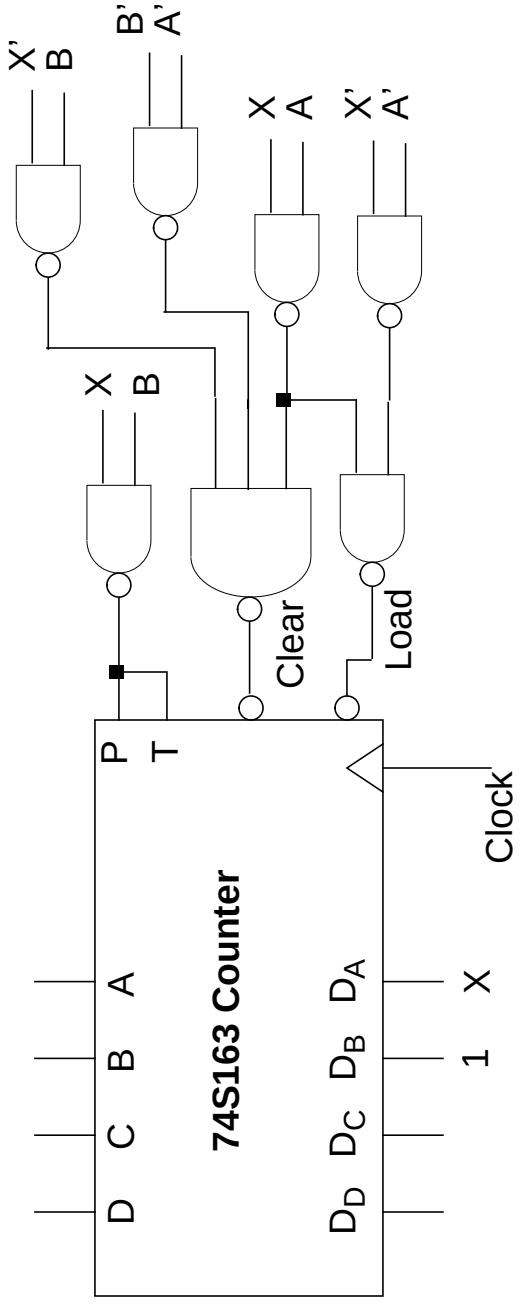


D_A =

X

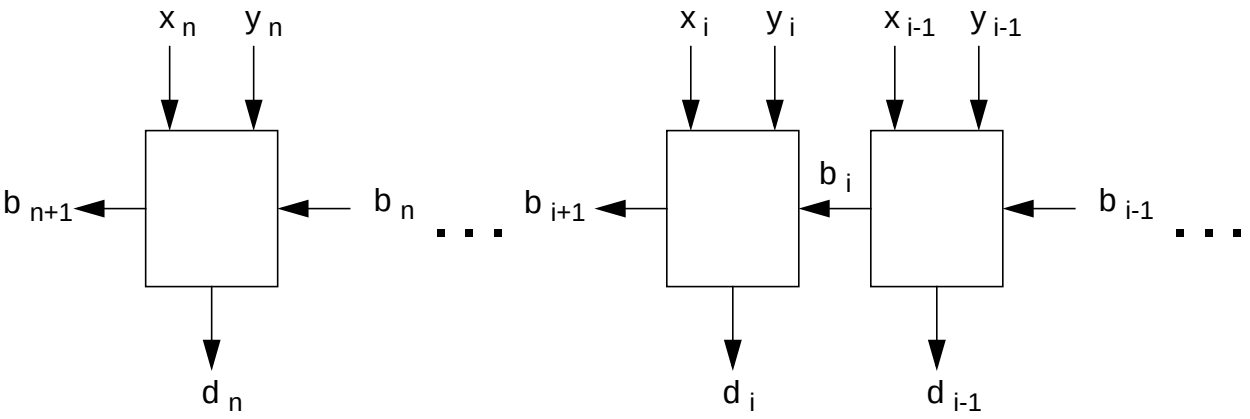
c) Draw the network diagram with the 74163 counter chip and the external logic gates to realize the network. Use only NAND gates for the realization of external logic.

Solution:



Problem No. 3:

Design a full subtracter as an iterative network. This network directly subtracts one n-bit binary number from the other, as displayed in the following diagram.



The i^{th} cell implements $d_i = x_i - y_i - b_i$ with b_{i+1} as the borrow to be propagated to the next cell.

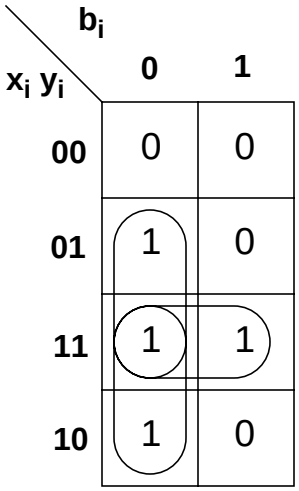
a) Derive the truth table for a typical cell for the direct full subtracter described above.

Solution:

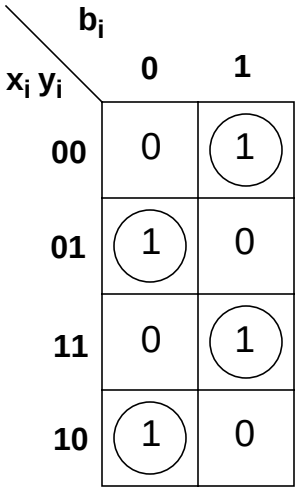
x_i	y_i	b_i	b_{i+1}	d_i
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

b) Draw the K-maps and derive equations for the design of a typical cell.

Solution:



$b_{i+1} = b'_i\ y_i + b'_i\ x_i + x_i\ y_i$



$d_i = b_i \oplus x_i \oplus y_i$

c) Describe how you will use the direct full subtracter described above if 2's complement logic is used to describe negative numbers.

Solution:

To use the direct full subtracter when a 2's complement logic is used, we first need to convert any negative numbers to their 2's complement and then use the direct subtraction. The result of the direct subtraction is converted back to 2's complement.