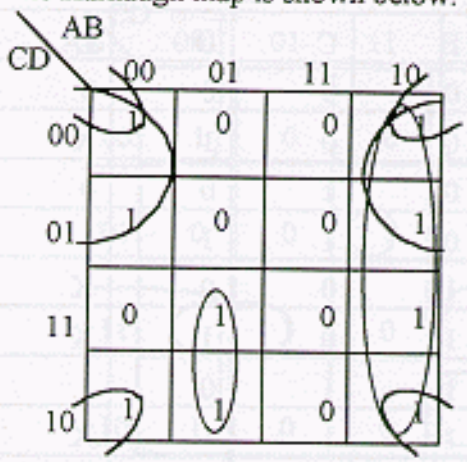
12.23

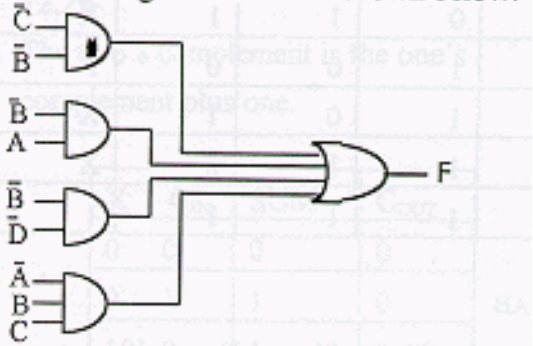
The Karnaugh map is shown below.



The map leads to the expression

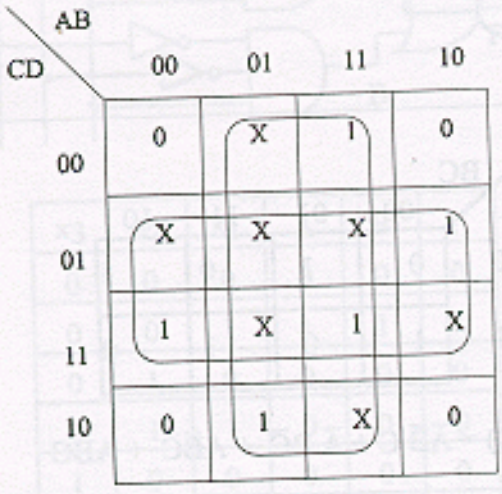
$$f = \bar{B}\bar{C} + A\bar{B} + \bar{A}BC + \bar{B}\bar{D}$$

and to the gate realization shown below.

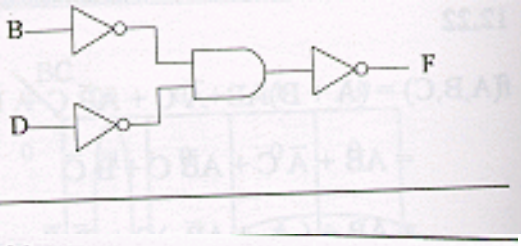


12.25

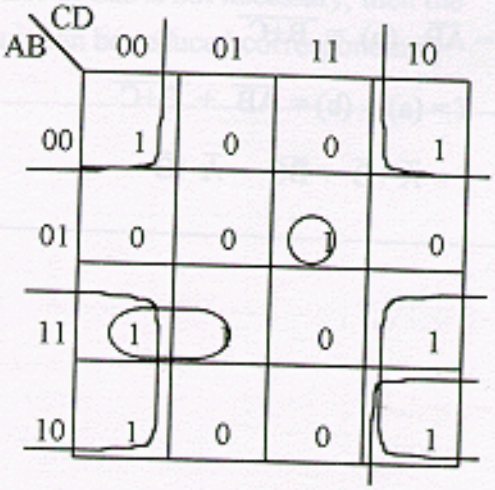
A	B	C	D	F
0	0	0	0	0
0	0	0	1	X
0	0	1	0	0
0	0	1	1	1
0	1	0	0	X
0	1	0	1	X
0	1	1	0	1
0	1	1	1	X
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	X
1	1	0	0	1
1	1	0	1	X
1	1	1	0	X
1	1	1	1	1



$F = B + D$



12.28



$F = \bar{B}\bar{D} + A\bar{D} + AB\bar{C} + \bar{A}BCD$

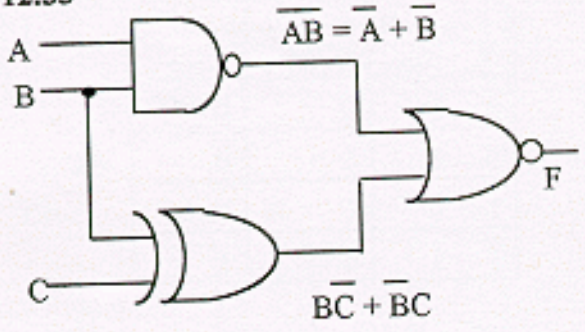
12.30

(a) $= \overline{AB}$ (b) $= \overline{B+C}$

$f = (a) + (b) = \overline{AB} + \overline{B+C}$

$= \bar{A} + \bar{B} + B\bar{C} = \bar{A} + \bar{B}$

12.33



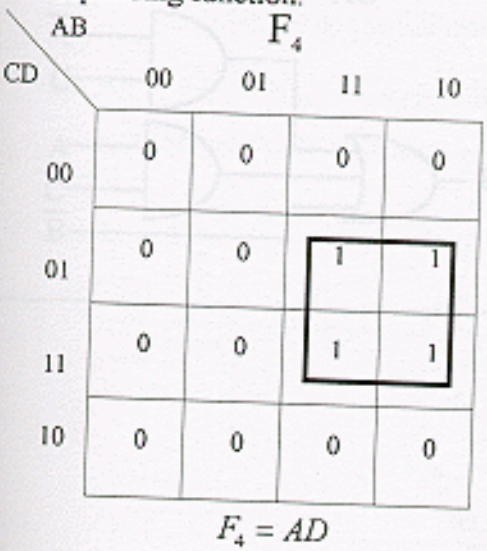
$f(A,B,C) = ABC$

12.36

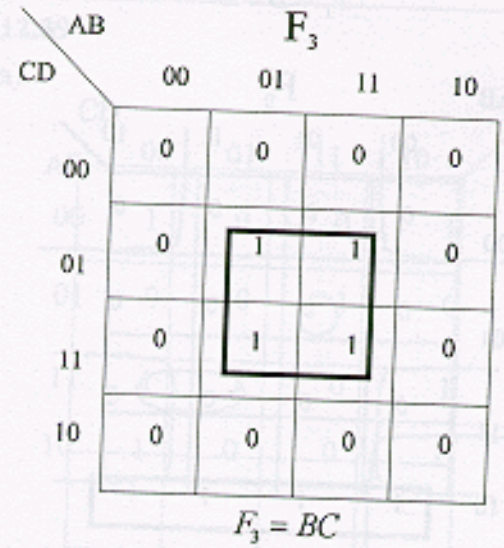
The appropriate truth table can be constructed as follows:

A B C D	F4	F3	F2	F1	F0
0 0 0 0	0	0	0	0	0
0 0 0 1	0	0	0	1	0
0 0 1 0	0	0	0	0	1
0 0 1 1	0	0	1	1	0
0 1 0 0	0	0	0	1	0
0 1 0 1	0	1	0	1	0
0 1 1 0	0	0	0	1	1
0 1 1 1	0	1	1	1	0
1 0 0 0	0	0	1	0	0
1 0 0 1	1	0	0	1	0
1 0 1 0	0	0	1	0	1
1 0 1 1	1	0	1	1	0
1 1 0 0	0	0	1	1	0
1 1 0 1	1	1	0	1	0
1 1 1 0	0	0	1	1	1
1 1 1 1	1	1	1	1	0

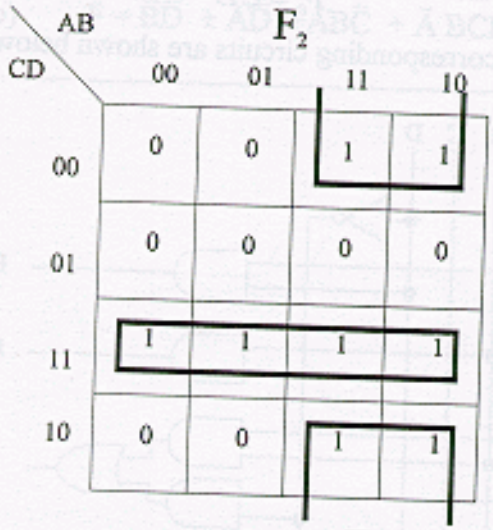
Next, we construct a Karnaugh map for each bit of the output, and determine its corresponding function.



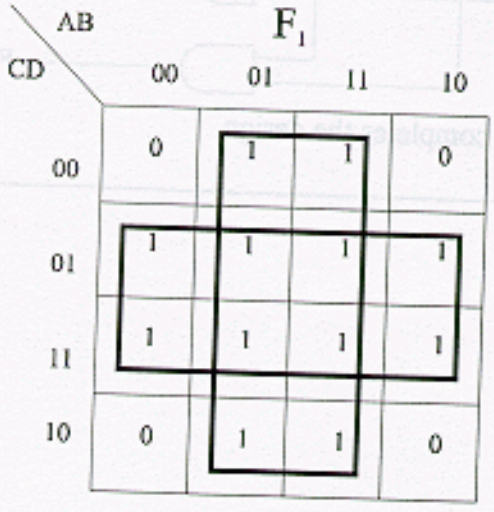
$F_4 = AD$



$F_3 = BC$



$F_2 = AB + A\overline{D}$



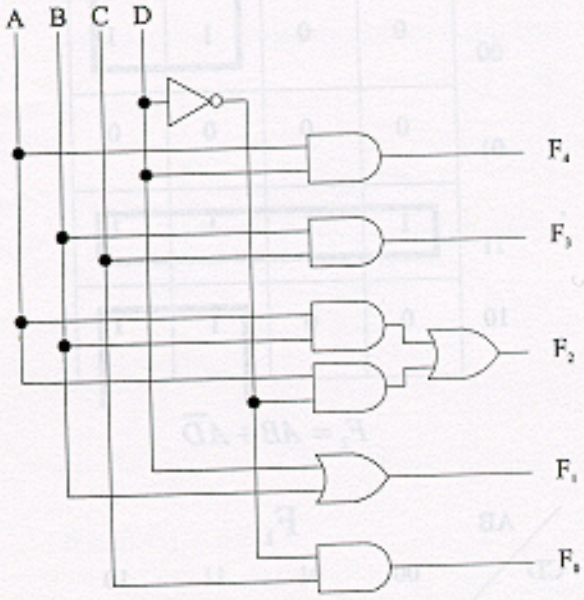
$F_1 = B + D$

F_0

CD \ AB	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	1	1	1	1

$F_0 = C\overline{D}$

The corresponding circuits are shown below:



This completes the design.

12.46

Assuming that the enable input (EN) is active high, when EN is logic 0 (A is logic 1), all decoder outputs of the first decoder are forced to logic 1 independent of the inputs. However, when EN is logic 1 (A is logic 0), all decoder outputs of the second decoder are forced to logic 1 independent of the select inputs. Therefore, A functions as the fourth bit of the select inputs. Thus, the circuit operates as a 4 of 16 decoder.

12.49

$f = \overline{A}B\overline{C} + A\overline{B}\overline{C} + AC$

BC \ A	0	1
00	0	1
01	0	1
11	0	1
10	1	0

From the truth table it is clear that:

$I_0 = 0$

$I_1 = \overline{C}$

$I_2 = 1$

and

$I_3 = C$