Name: _____

Problem	Points	Score
1a	10	
1b	10	
2	10	
3a	10	
3b	10	
3c	10	
4a	10	
4b	10	
4c	10	
4d	10	
Total	**100**	

Notes:

1. The exam is closed book / closed notes. You are allowed a copy sheet — only **one** side of **one** standard US-size (8.5” x 11”) sheet of paper — on which you can write relevant information such as equations. You are allowed to bring copy sheets from previous exams.

2. Please show **all** work. Incorrect answers with no supporting explanations or work will be given no partial credit.

3. If I cannot read or follow your solution, it is wrong; and no partial credit will be given — **PLEASE BE NEAT**!

4. Please indicate clearly your answer to every problem.

5. There is sufficient space after each problem to write your solution. In case you need extra paper please see the instructor.

6. Show complete work and detailed steps for proper credit.

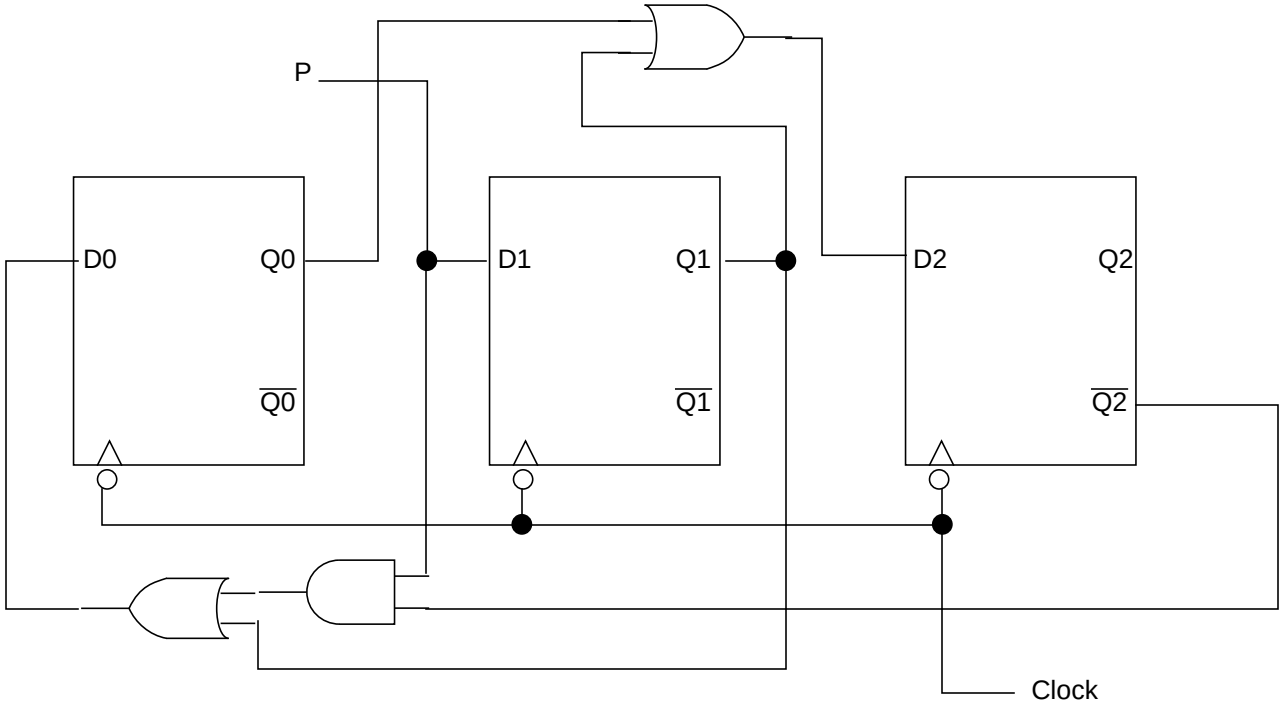
Problem No. 1:

A synchronous sequential digital circuit with three negative edge-triggered D flip-flops has an external input P. The circuit is designed as follows —

$$D_0 = P\overline{Q_2} + Q_1$$
$$D_1 = P$$
$$D_2 = Q_0 + Q_1$$

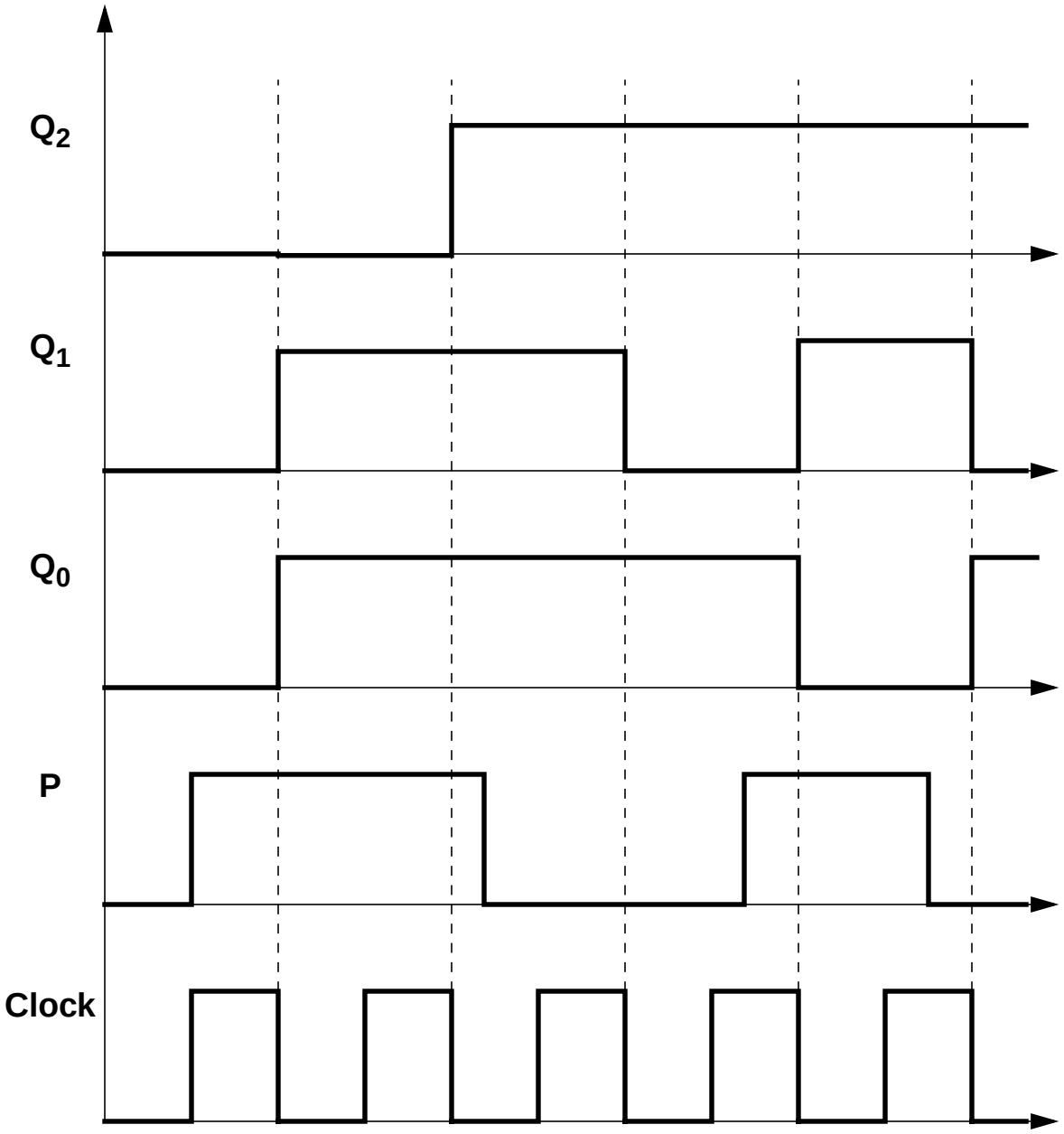
a) Draw the circuit diagram.

Solution:



b) Complete the following timing diagram.

Solution:



Problem No. 2:

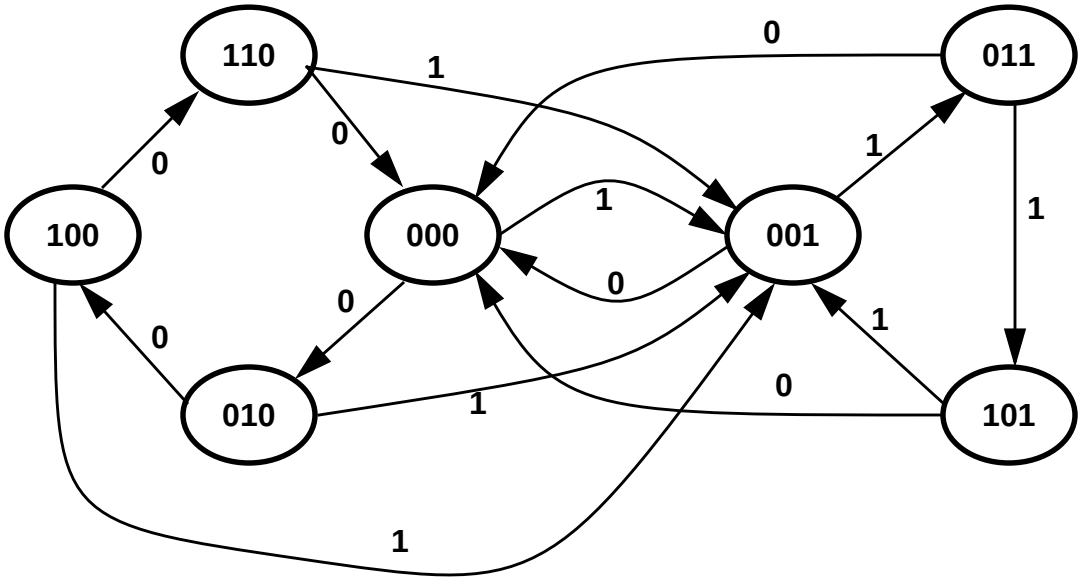
A sequential digital circuit counts successive even or odd numbers between 0 and 6, inclusive. If the control input P is 0, the circuit goes through the even numbers starting from 0. If P is 1, the circuit enumerates the odd numbers starting from 1. If the maximum even (odd) value is reached in either case, the circuit restarts from the smallest even (odd) number.

How many flip-flops are required to implement this circuit? Draw a state transition diagram to illustrate the working of this circuit.

Solution:

Since there are a total of 7 states corresponding to each number to be counted, the number of flip-flops required is 3.

A state diagram is as follows:



Problem No. 3:

An instrumentation amplifier is designed with the following parameters —

$$V_{a,\,dif} = 0.6mV \qquad R_1 = 10k\Omega \qquad R = 1k\Omega$$
$$V_{b,\,dif} = 0.4mV \qquad R_2 = 10k\Omega$$
$$V_{com} = 0.5mV \qquad R_F = 5k\Omega \qquad \Delta R = 5\%$$

a) Find the differential mode output voltage $V_{out,dif}$.

Solution:

We have the differential mode output voltage

$$V_{\text{out,diff}} = \frac{R_F}{R}\frac{R_F + R}{R_F + R + \Delta R}AV_{\text{a,diff}} - \frac{R_F}{R}AV_{\text{b,diff}}$$

where

$$A = 1 + \frac{2R_2}{R_1} = 1 + \frac{2 \times 10\text{k}\Omega}{10\text{k}\Omega} = 3$$

Therefore by substituting appropriate values, we get

$$V_{\text{out,diff}} = \frac{5\text{k}\Omega}{1\text{k}\Omega} \times \frac{5\text{k}\Omega + 1\text{k}\Omega}{5\text{k}\Omega + 1\text{k}\Omega + 0.05\text{k}\Omega} \times 3 \times 0.6\text{mV} - \frac{5\text{k}\Omega}{1\text{k}\Omega} \times 3 \times 0.4\text{mV}$$
$$= 2.926\text{mV}$$

b) Find the common mode output voltage $V_{out,com}$.

Solution:

We have the common mode output voltage

$$V_{\text{out,com}} = \frac{R_F}{R}\left(\frac{R_F + R}{R_F + R + \Delta R} - 1\right)AV_{\text{com}}$$

where

$$A = 3$$

as obtained in part **a)**.

Therefore by substituting appropriate values, we get

$$\begin{aligned} V_{\text{out,com}} &= \frac{5\text{k}\Omega}{1\text{k}\Omega} \times \left(\frac{5\text{k}\Omega + 1\text{k}\Omega}{5\text{k}\Omega + 1\text{k}\Omega + 0.05\text{k}\Omega} - 1\right) \times 3 \times 0.5\text{mV} \\ &= 0.062\text{mV} \end{aligned}$$

c) Find the common mode rejection ratio in dB based on your answers to parts **a)** and **b)**.

Solution:

The common mode rejection ration in dB is given by

$$\begin{aligned} CMRR_{\text{dB}} &= 20\log_{10}\left|\frac{A_{\text{out,diff}}}{A_{\text{out,com}}}\right| \\ &= 20\log_{10}\left|\frac{V_{\text{out,diff}}/(V_{\text{a,diff}} - V_{b,\text{diff}})}{V_{\text{out,com}}/V_{\text{com}}}\right| \\ &= 20\log_{10}\left|\frac{2.926\text{mV}/(0.6\text{mV} - 0.4\text{mV})}{0.062\text{mV}/0.5\text{mV}}\right| \\ &= 41.44\text{dB} \end{aligned}$$

Problem No. 4:

Design a 3-bit digital-to-analog converter (DAC) with R_0 = 12kΩ, and an analog voltage range 0-15V using a summing amplifier design. Assume that a 1 bit corresponds to 5V, and a 0 bit corresponds to 0V.

a) Find the voltage increment size δV.

Solution:

The voltage increment size depends on the analog voltage range and the number of bits. We have

$$\delta V = \frac{V_{\text{a,max}}}{2^n - 1} = \frac{15V}{2^3 - 1} = 2.143V$$

b) Find the value of R_F necessary to build this DAC and draw a circuit diagram.

Solution:

The feedback resistance value depends on the voltage increment size and the digital voltage levels, as well as the input resistance. We have

$$\delta V = V_{in}\frac{R_F}{R_0}$$

$$\therefore R_F = \frac{R_0 \times \delta V}{V_{in}}$$

$$= \frac{12\text{k}\Omega \times 2.143V}{5V}$$

$$= 5.143\text{k}\Omega$$

c) Find the analog output for the binary digital value 110 using the DAC designed in parts **a)** and **b)**.

Solution:

The analog value for a given digital bit sequence is given by

$$\begin{aligned} V_a &= \delta V \sum_{i=0}^{n-1} 2^i b_i \\ &= 2.143V \times (2^2 \times 1 + 2^1 \times 1 + 2^0 \times 0) \\ &= 2.143V \times 6 \\ &= 12.857V \end{aligned}$$

d) What is the minimum number of bits required to digitize an analog signal with a resolution of 8%? What resolution can one get by using 5 bits?

Solution:

For a minimum resolution of 8%, we have the number of bits given by

$$2^{-n} < 0.08$$
$$\therefore n > 3.64$$

Thus 4 bits are required.

If 5 bits are used, then the resolution is given by

$$2^{-5} = 0.03125 = 3.125\%$$