An EEG Artifact Detection and Removal Technique for Embedded Processors

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Neurophysiological signals such as Electroencephalogram (EEG) can be used in a variety of purposes including detecting fatigue, stress, brain disorders, brain-computer interfaces (BCIs), or building better models of human variability and human brain. However, EEG signal is frequently defiled with other electrical sources not related to brain activity. These artifacts may emerge from external sources such as eye blinks, muscle & head movement, and power lines. Existing techniques for removing artifacts such as independent component analysis (ICA) are highly computationally intensive and need to process data offline due in large part to the highly volatile, non-stationary nature of the brain signals, especially in natural, noise-ridden environments.

In this paper, we propose a software-hardware real time solution for receiving, pre-processing, artifact detection and removal in real-time suitable for lightweight wearable devices. This is accomplished through two steps: 1) Flexible online deployment of artifact detection by utilizing simple feature extraction techniques and machine learning classifiers and 2) Artifact removal by implementing discrete wavelet transform (DWT) in cascade to decompose the signal for final thresholding without rejecting any essential brain information. The contributions of this paper include automatic artifact detection and removal while decreasing computational complexity and memory requirements in online fashion. Moreover, our technique does not require large data-set for removing artifacts in contrast with existing popular ICA based solution. As the proposed system is automatic and online, it is more suitable than existing techniques for wearable devices and real-time BCI applications.

The proposed architecture is based on an input/output buffer, data pre-processing unit, artifact detection unit and finally, artifact removal unit. To detect the artifact in a window of EEG signal, we have implemented k-nearest neighbor classifiers (KNN), support vector machines (SVM) with linear kernel and logistic regression (LR) in online fashion. The features such as area under the wave, normalized decay, mean energy, average peak amplitude, and average valley amplitude are obtained for each EEG channel using a 1 Sec window with sampling rate of 512 Hz. KNN outperforms LR and SVM to detect artifacts in terms of all statistical measures such as sensitivity, specificity, accuracy, and F-measure. The artifact removal unit consists of three main blocks: cascaded DWT blocks up to level 8 to decompose input signal, median filter for thresholding selected coefficients, and inversely cascaded iDWT blocks to reconstruct clean EEG signal. Artifacts such as eye blinks are localized only in the DWT coefficients of low-frequency subbands and a higher order median filter is applied only to the chosen low-frequency coefficients to threshold the amplitude without expelling vital data from EEG.

Finally, our proposed architecture is implemented with a trained artifact detector unit on an ARM Cortex-A53 embedded processor which provides a balance between performance, power-efficiency, and cost. Our proposed technique can operate and process 1 Sec window of EEG signal with 512 Hz sample rate in less than one second and is ready to take next second of EEG signal. We present the overall system, with preliminary results for software and hardware implementation when using real EEG data. The method outperforms the more common ICA based solution in terms of computational complexity and memory requirements. Finally, the entire architecture can execute on ARM Cortex-A53 embedded processor running at 1.2 GHz with average power consumption of 1.5 W within 0.94 Sec processing time. In contrast, with the least amount of samples ICA needs to converge, ICA based solution requires around 30 Sec on the embedded processor running at same clock speed.

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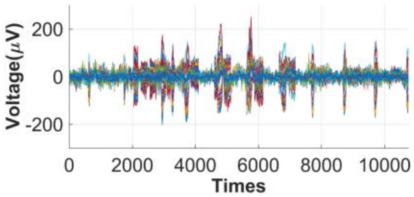
Abstract: A fully online and automated artifact detection and removal software-hardware embedded technique for the electroencephalogram (EEG) is developed for a variety of purposes such as brain-computer interfaces, disease diagnosis, and determining cognitive states. The proposed system is based upon machine learning classifiers, including K-Nearest Neighbors (KNN), Logistic Regression (LR), and Support Vector Machine (SVM) to detect artifacts and wavelet decomposition by cascaded discrete wavelet transform (DWT) to remove artifacts from EEG signal. Our proposed system is able to operate and process 1 Sec window of EEG signal with 512 Hz sample rate in less than one second. We present the overall technique, with preliminary results for software and hardware implementation when using real EEG data recordings. The method outperforms the more common ICA based solution in terms of computational complexity and memory requirements. Finally, the entire architecture is implemented on ARM Cortex-A53 embedded processor running at 1.2 GHz and consumes average power of 1.5 W within 0.94 Sec processing time. In contrast, with the least amount of samples ICA needs to converge, ICA based solution requires around 30 Sec on the embedded processor running at same clock speed.

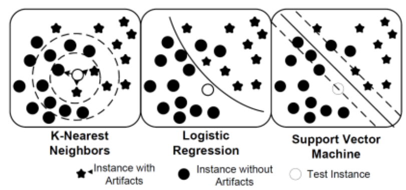
Proposed Technique

Our proposed technique consists of three units:
Data Pre-processing: Filtering such as high pass filter and notch filter to suppress non-EEG frequency component. Also, mean normalization is applied to expel the chance of biased features. The figure below shows the butterfly plot of all channels after pre-processing.

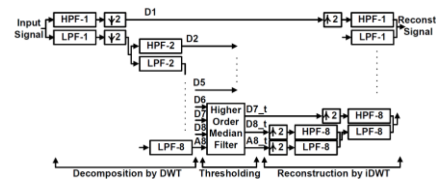


Key Features of Our Proposed Technique:
- Online artifact detection & removal while decreasing computational complexity & memory requirements
- No requirement of large EEG data samples
- Suitable for wearable devices and real-time BCI applications as it is online, real-time and low power
- Implemented and verified on low-power and small embedded processor such as ARM Cortex-A53 CPU

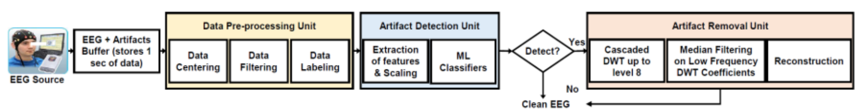
Artifact Detection: We evaluate the performance of KNN, SVM with linear kernel and logistic regression to detect artifact. The features such as area under the wave, normalized decay, mean energy, average peak amplitude, and average valley amplitude are obtained for each channel from 1 Sec window of EEG signal.



Artifact Removal: This unit consists of three main blocks: cascaded DWT blocks up to level 8 to "**decompose**" input signal, median filter for "**thresholding**" selected coefficients, and inversely cascaded iDWT blocks to "**reconstruct**" clean EEG signal which is shown on the below figure.

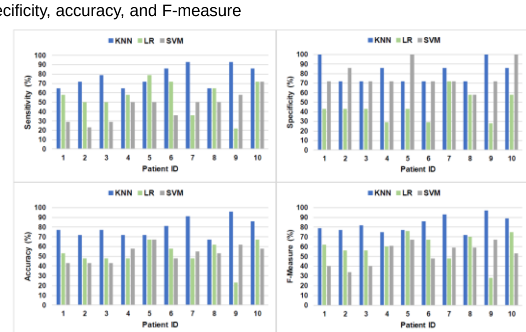


Our entire proposed architecture is shown below:

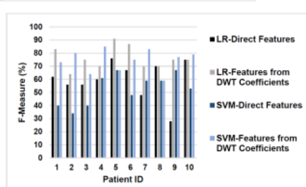


Software Analysis

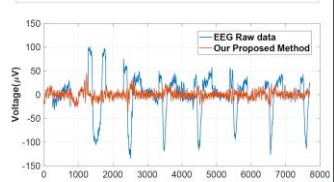
- Comparison of the performance of three classifiers: KNN, LR and SVM with the linear kernel for the detection of artifacts in EEG is shown below.
- KNN outperforms LR and SVM in terms of all statistical measures: sensitivity, specificity, accuracy, and F-measure



- Performance of the other two classifiers, LR & SVM, is improved by expanding the dimension of feature vectors using DWT in cascade which is shown on the right.
- Improvement of is done by extracting features from all DWT coefficients rather than direct feature extraction.



- Visualization of artifact removed reconstructed clean EEG by our proposed technique on the right figure
- All the eye blinks and/or eye movement artifacts are eliminated and EEG information remains protected in the reconstructed clean EEG.



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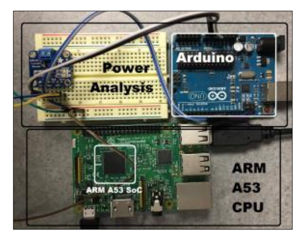
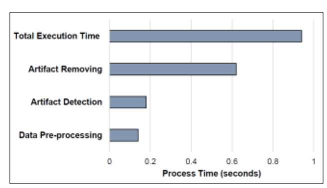
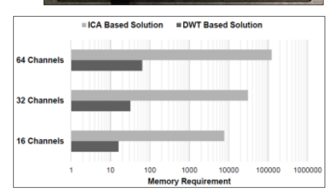
Hardware Implementation Results & Comparison

- Our proposed technique outperforms ICA based solutions in terms of process time and memory requirements on embedded processor.
- Implemented on ARM Cortex-A53 embedded processor running at 1.2 GHz with average power consumption of 1.5 W within 0.94 Sec processing time

- Power measurement set up: Power measurement of ARM Cortex A-53 CPU is completed using TI INA219 voltage and power IC sampled by an Arduino Uno.
- In contrast, with the least amount of samples ICA needs to converge, ICA based solution requires around 30 Sec on the same processor running at same clock speed.







Process Time: Breakdown of the process time for data processing, artifact detection and removing: The entire DWT based architecture can be executed in less than 1 Sec (precisely 0.94 Sec) on Cortex-A53 CPU running at 1.2 GHz.

Memory requirement: Comparison for number of memory requirements between ICA based solution and DWT based solution in log-scale. DWT based system requires 2 to 3 orders of magnitude less memory compared to ICA based solution.

References

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